RF Power Field Effect Transistor

DSM09S007D1

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Rev. 1, 3/2018

N-ChannelEnhancement-ModeMOSFET

Designedfor handheldtwo–wayradioapplicationswithfrequencies from136to941 MHz. The high gain,ruggedness andBroadbandperformance ofthisdevicemake it idealforlarge–signal,common–source amplifier applications inhandheldradioequipment.

136-941MHz, 7.0W, 7.5V

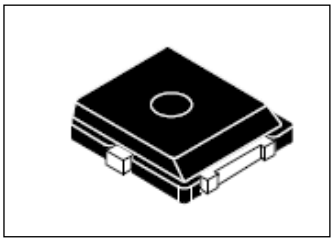
BROADBAND RF

POWERTRANSISTOR

Typical Broadband EVB Performance(I_{DQ}=200mA, T_A = 25℃, CW)

Freq.	V_{GS}	V_{DS}	Gmax	Pout		PAE
[MHz]	[V]	[V]	[dB]	[dBm]	[Watts]	[%]
440	2.3	6.5	21.1	38.5	7.1	68.9
		7.5	21.2	39.6	9.1	68.9
		8.5	21.4	40.6	11.4	68.3

- Capable ofHandling20:1 VSWR@ 7.5Vdc,7.0Watts, CW



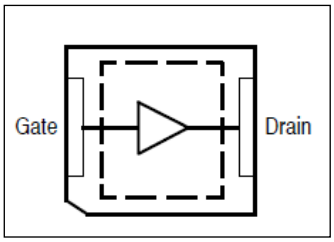


Figure 1. Pin Connections

Features

- Characterized for Operation from 136 to 941 MHz
- Unmatched Input and Output Allowing Broad Frequency Range Utilization
- Integrated ESD Protection
- Broadband – Full Power Across the Band
- Exceptional Thermal Performance
- Extreme Ruggedness

Typical Applications

- Output Stage VHF Band Handheld Radio
- Output Stage UHF Band Handheld Radio
- Output Stage for 700–800 MHz Handheld Radio
- Driver for 10–1000 MHz Applications

Table1.MaximumRatings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +30	Vdc
Gate-Source Voltage	V_{GS}	–5.0, +8	Vdc
Operating Voltage	V_{DD}	0, +12	Vdc
Storage TemperatureRange	T_{stg}	–65 to +150	℃
Case Operating Temperature	T_C	–40 to +150	℃
Operating JunctionTemperature	T_J	–40 to +150	℃
Power Dissipation @TC=25℃	PD	30	W

Table 3.ESD Protection Characteristic

Test Methodology	Class
Human Body Model (per JESD22--A114)	2, passes 2500 V
Machine Model (per EIA/JESD22--A115)	A, passes 100 V
Charge Device Model (per JESD22--C101)	IV, passes 2000 V

Table 4. Electrical Characteristics (T_A=25℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ.	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS}=5Vdc,V_{DS}=0Vdc)	I_{GSS}	-	-	1	nAdc
ZeroGateVoltage DrainLeakageCurrent (V_{DS}=30Vdc,V_{GS}=0Vdc)	I_{DSS}	-	-	2	μAdc
ZeroGateVoltage DrainLeakageCurrent (V_{DS}=7.5Vdc,V_{GS}=0Vdc)	I_{DSS}	-	-	1	μAdc
On Characteristics					
GateThresholdVoltage(V_{DS}=10Vdc,I_D=1mA)	$V_{GS(th)}$	1.5	1.9	2.4	Vdc
Gate QuiescentVoltage(V_{DD}=7.5Vdc, I_D=200mAMeasuredin FunctionalTest)	$V_{GS(Q)}$	1.7	2.3	2.8	Vdc
Drain-SourceOn-Voltage(V_{GS}=5Vdc,I_D=100mA)	$V_{DS(ON)}$	-	0.04	-	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (VDG=7.5V, Level=50mVac@1MHz)	Crss	-	2.2	-	pF
Output Capacitance (VDS=7.5V,Level=50mVac@1MHz)	Coss	-	16	-	pF
Input Capacitance (VGS=0V,Level=50mVac@1MHz)	Ciss	-	70	-	pF

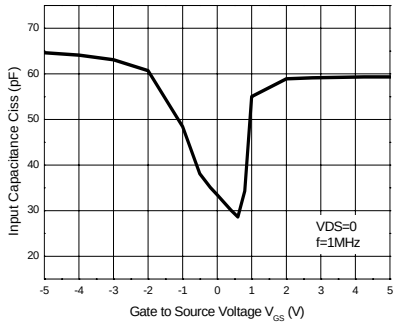
Typical Performances (In DuSemi Narrowband Test DEMO,50 Ohm system)

Frequency=440MHz, VDD=7.5Vdc, I_{DQ}=200mA, T_A=25℃

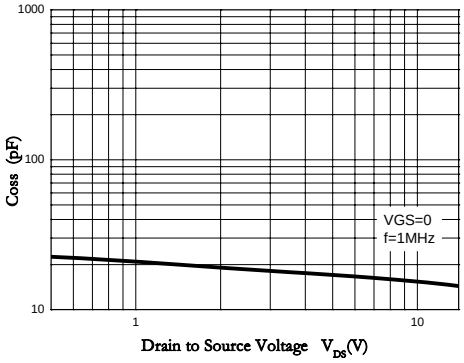
Output Power	P_{out}	-	9	-	Watts
PowerGain	G_{PS}	-	21	-	dB
DrainEfficiency	η_D	-	68	-	%

Main Characteristics

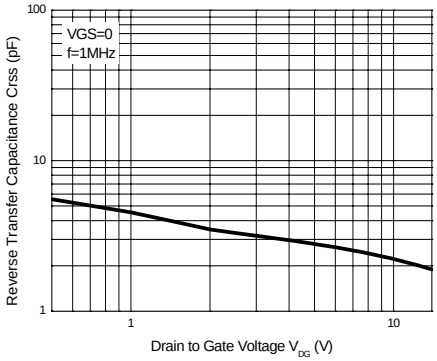
Input Capacitance Curve



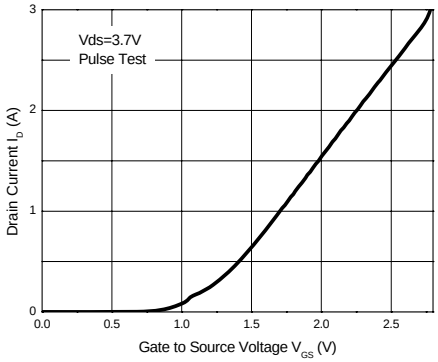
Output Capacitance Curve



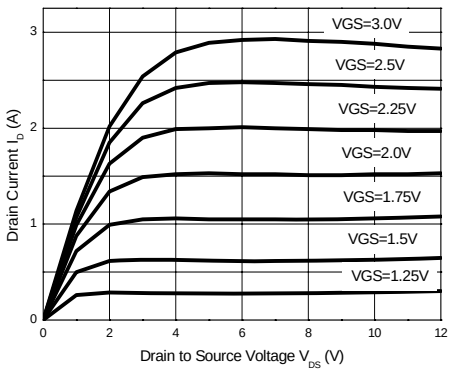
Reverse Transfer Capacitance Curve



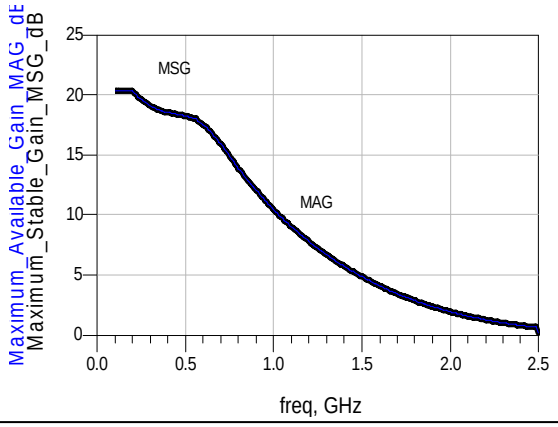
Transfer Characteristic Curve



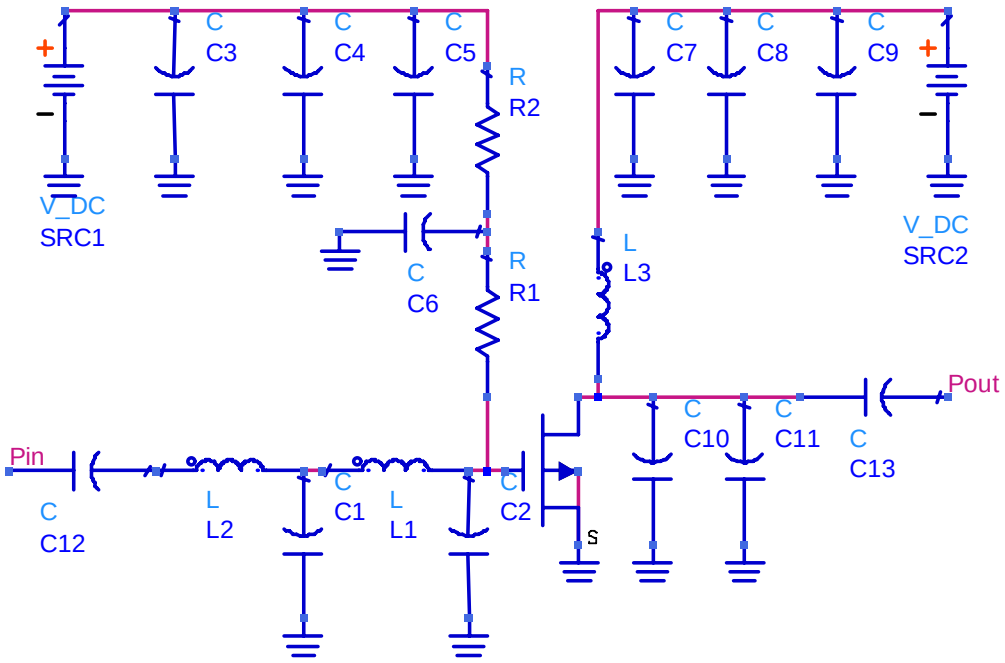
DC Output Characteristic Curve



MSG & MAG Curve



Broad Band EvaluationCircuit (@VDD=7.5V, f =460MHz)



Test Circuit ComponentLayout

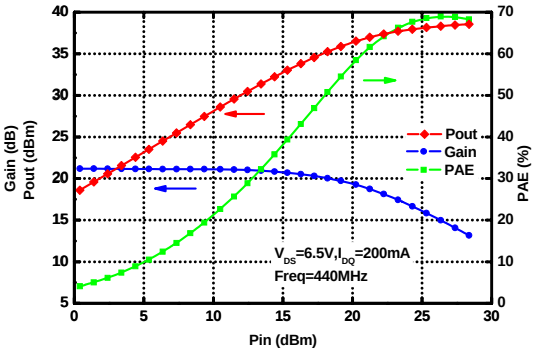
Table5. TestCircuitComponentDesignationsand Value

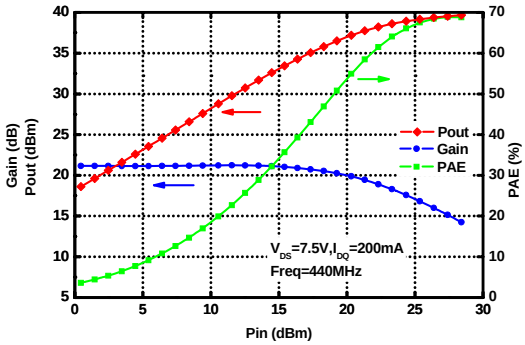
Part	Description	PartNumber	Manufacturer
R1	470Ohm	—	—
R2	6.8KOhm	—	—
L1, L2	3.9nH	—	—
L3	8 Turns D: 0.5 mm, φ 2.4 mm Enamel Wire	—	—
C5, C6, C7, C12, C13	100pF Chip Capacitors	GQM21P5C1H101JB01	Murata
C1, C2	18pF Chip Capacitors	GRM1885C1H201JA01	Murata
C4, C8	1000pF Chip Capacitors	GRM1885C1H102JA01	Murata
C3, C9	10uF,25VChip Capacitors	—	—
C10	9pF Chip Capacitors	—	Murata
C11	4.3pF Chip Capacitors	—	Murata
PCB	FR-4 ,1.6mm, ε_r4.5	—	—

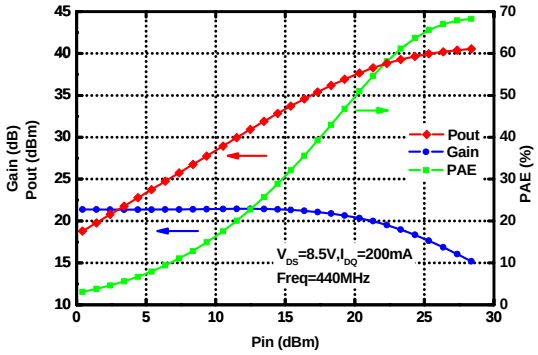
TYPICAL CHARACTERISTICS

1.440MHz @ V_{DS}, Pout, Gain, PAE vs. Pin

Freq	V_{GS}	V_{DS}	Pout		Gain	PAE
[MHz]	[V]	[V]	[dBm]	[Watts]	[dB]	[%]
440	2.3	6.5	38.5	7.1	21.1	68.9
		7.5	39.6	9.1	21.2	68.9
		9.0	40.6	11.4	21.4	68.3

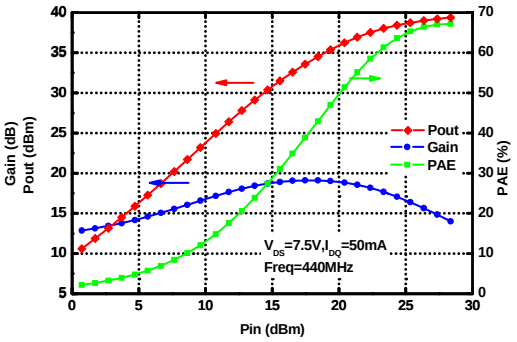


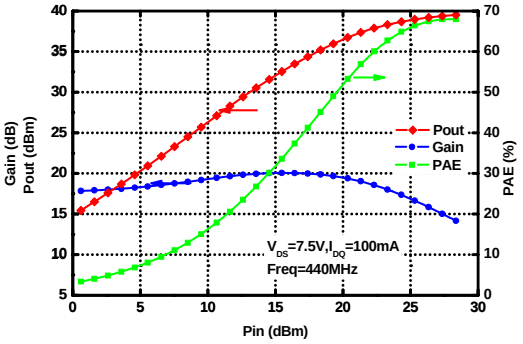


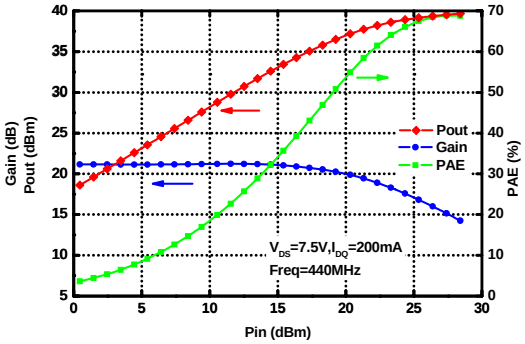


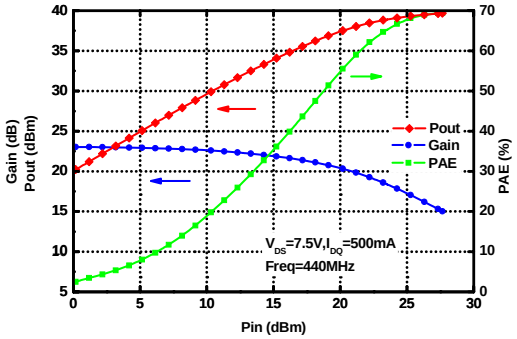
2.440MHz @ V_{GS}, Pout, Gain, PAE vs. Pin

Freq	V_{DS}	I_{DQ}	Pout		Gain	PAE
[MHz]	[V]	[mA]	[dBm]	[Watts]	[dB]	[%]
440	7.5	50	39.4	8.7	19.1	67.2
		100	39.5	8.9	20.0	68.0
		200	39.6	9.1	21.2	68.9
		500	39.7	9.3	23.1	69.4



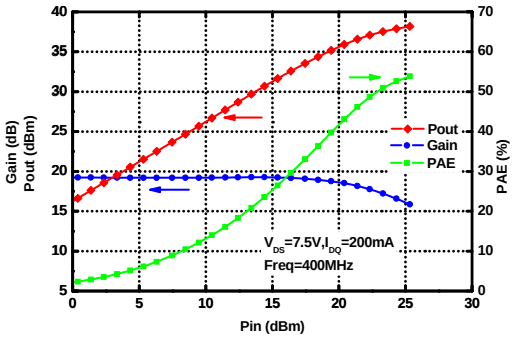


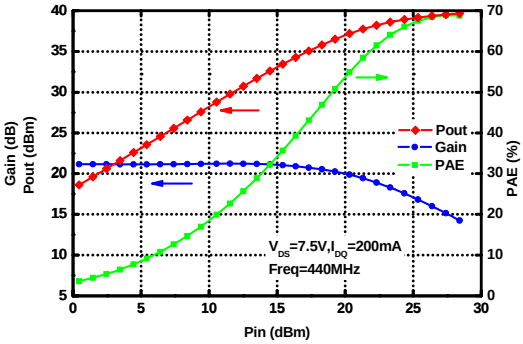


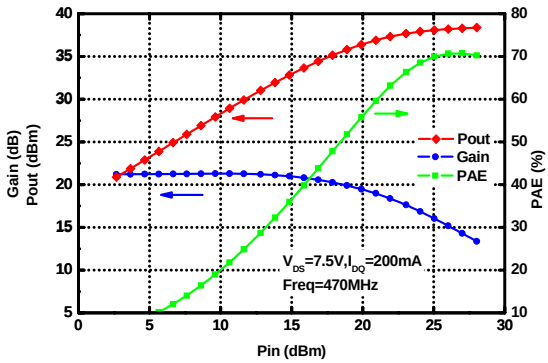


3. 7.5V @ Frequency, Pout, Gain, PAE vs. Pin

V_{DS}	Freq	Pout		Gain	PAE
[V]	[MHz]	[dBm]	[Watts]	[dB]	[%]
7.5	400	39.1	8.1	19.3	59.3
	440	39.6	9.0	21.4	68.9
	470	38.5	7.0	21.3	70.7

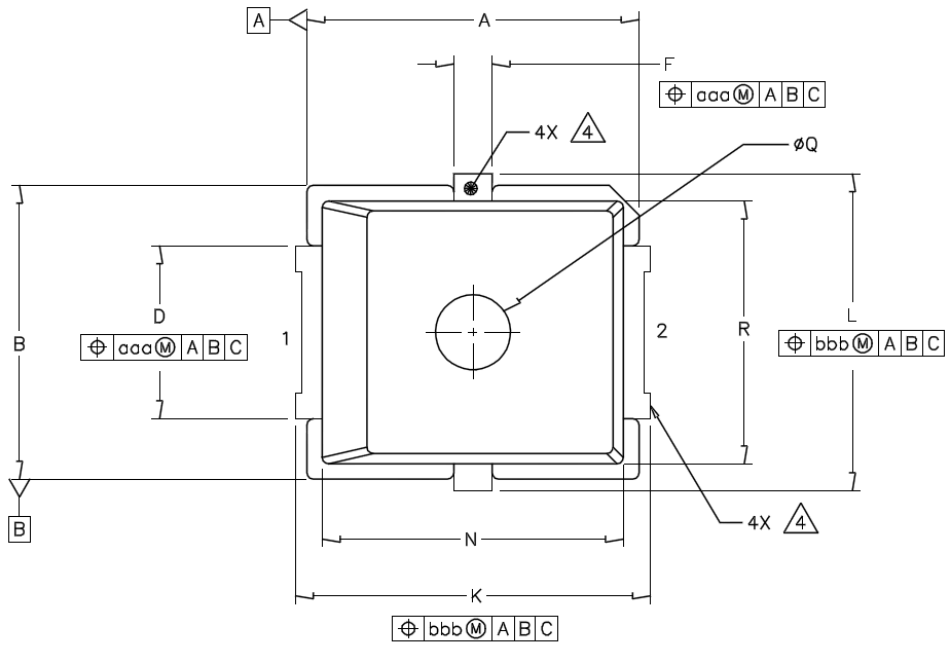




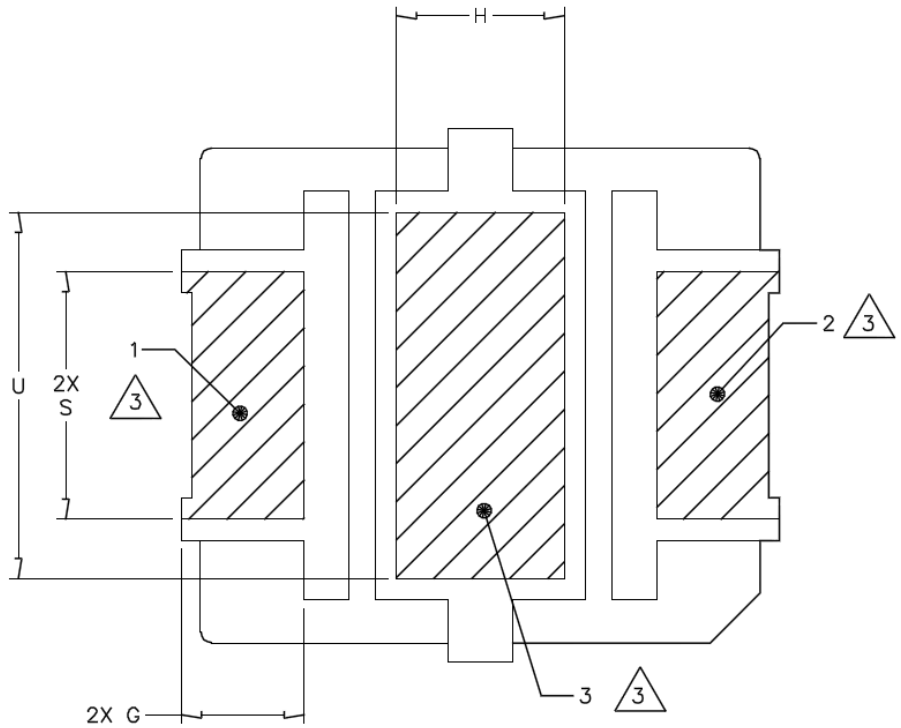


PACKAGE

PACKAGE DIMENSIONS



PCB Pad Layout for PLD



Bottom View

PACKAGEDIMENSIONS

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.255	.265	6.48	6.73	Q	.055	.063	1.40	1.60
B	.225	.235	5.72	5.97	R	.200	.210	5.08	5.33
C	.065	.072	1.65	1.83	S	.110	–	2.79	–
D	.130	.150	3.30	3.81	U	.156	–	3.96	–
E	.021	.026	0.53	0.66	aaa		.004		0.10
F	.026	.044	0.66	1.12	bbb		.005		0.13
G	.038	–	0.97	–					
H	.069	–	1.75	–					
J	.160	.180	4.06	4.57					
K	.273	.285	6.93	7.24					
L	.245	.255	6.22	6.48					
N	.230	.240	5.84	6.10					
P	.000	.008	0.00	0.20					

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
1	March 2018	Initial Release of Data Sheet