RF Power Field Effect Transistor

DSM09S005N

Document Number: DSM09S005N
Rev. 1, 5/2018

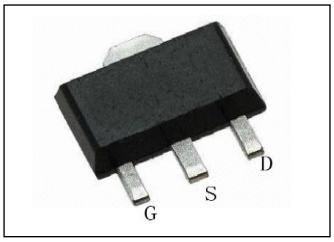
N-Channel Enhancement-Mode MOSFET

Designed for handheld two–way radio applications with frequencies from 136 to 941 MHz. The high gain, ruggedness and Broadband performance of this device make it ideal for large–signal, common–source amplifier applications in handheld radio equipment.

136–941 MHz, 5.0W, 7.5 V
BROADBAND RF
POWER TRANSISTOR

Typical Broadband EVB Performance (I_{DQ}=300mA, T_A = 25℃, CW)

V_{DD}	Freq.	Gmax	Pout		PAE
[V]	[MHz]	[dB]	[dBm]	[Watts]	[%]
7.5	400	20.4	38.0	6.3	56.9
	430	20.9	38.9	7.7	60.1
	440	21.5	39.3	8.5	63.4
	460	21.8	39.2	8.3	67.8
	480	20.9	38.0	6.3	67.2



- Capable of Handling 20:1 VSWR @7.5Vdc, 5.0Watts, CW

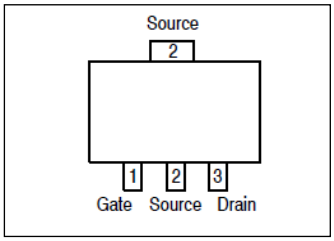


Figure 1. Pin Connections

Features

- Characterized for Operation from 136 to 941 MHz
- Unmatched Input and Output Allowing Broad Frequency Range Utilization
- Integrated ESD Protection
- Broadband – Full Power Across the Band
- Exceptional Thermal Performance
- Extreme Ruggedness

Typical Applications

- Output Stage VHF Band Handheld Radio
- Output Stage UHF Band Handheld Radio
- Output Stage for 700–800 MHz Handheld Radio
- Driver for 10–1000 MHz Applications

Table1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +20	Vdc
Gate-Source Voltage	V_{GS}	–5.0, +8	Vdc
Operating Voltage	V_{DD}	0, +12	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	℃
Case Operating Temperature	T_C	–40 to +150	℃
Operating Junction Temperature	T_J	–40 to +150	℃
Power Dissipation @TC=25℃	PD	20	W

Table2. ESD Protection Characteristic

Test Methodology	Class
Human Body Model (per JESD22--A114)	2, passes 2500 V
Machine Model (per EIA/JESD22--A115)	A, passes 100 V
Charge Device Model (per JESD22--C101)	IV, passes 2000 V

Table3. Electrical Characteristics (T_A=25℃ unless otherwise noted)

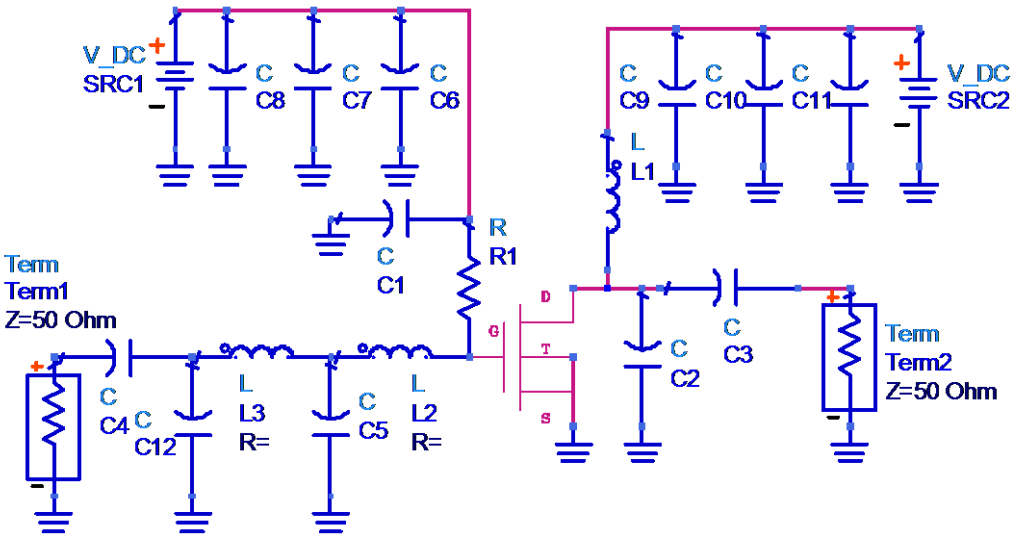
Characteristic	Symbol	Min	Typ.	Max	Unit
Off Characteristics					
Gate-Source Leakage Current (V_{GS}=5Vdc, V_{DS}=0Vdc)	I_{GSS}	-	-	1	uAdc
Zero Gate Voltage Drain Leakage Current (V_{DS}=20Vdc, V_{GS}=0Vdc)	I_{DSS}	-	-	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS}=7.5Vdc, V_{GS}=0Vdc)	I_{DSS}	-	-	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS}=7.5Vdc, I_D=1mA)	$V_{GS(th)}$	1.4	1.9	2.5	Vdc
Gate Quiescent Voltage (V_{DD}=7.5Vdc, I_D=300mA Measured in Functional Test)	$V_{GS(Q)}$	1.6	2.3	3.0	Vdc
Drain-Source On-Voltage (V_{GS}=5Vdc, I_D=100mA)	$V_{DS(ON)}$	-	0.05	-	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DG}=7.5V, Level=30mVac@1MHz)	Crss	-	2.1	-	pF
Output Capacitance (V_{DS}=7.5V, Level=30mVac@1MHz)	Coss	-	15.1	-	pF
Input Capacitance (V_{GS}=5V, Level=30mVac@1MHz)	Ciss	-	76	-	pF

Typical Performances (In DuSemi Narrowband Test DEMO, 50 Ohm system)

Frequency=460MHz, V_{DD}=7.5Vdc, I_{DQ}=300mA,T_A=25℃

Output Power	P_{out}	-	7.0	-	Watts
Power Gain	G_{PS}	-	21	-	dB
Drain Efficiency	η_D	-	67	-	%

Broad Band Evaluation Circuit (@VDD = 7.5V, f = 460 MHz)



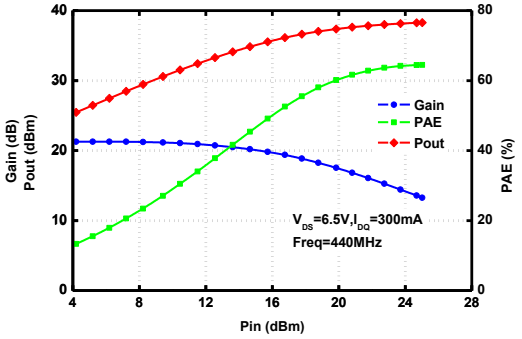
Test Circuit Component Layout

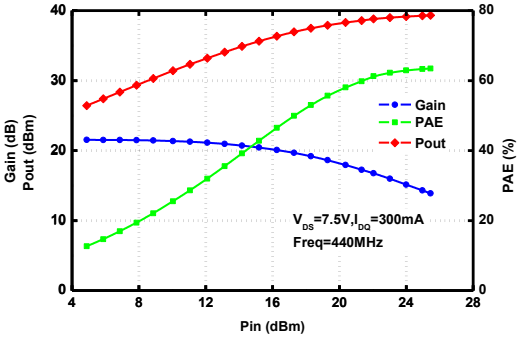
Table 4. Test Circuit Component Designations and Value

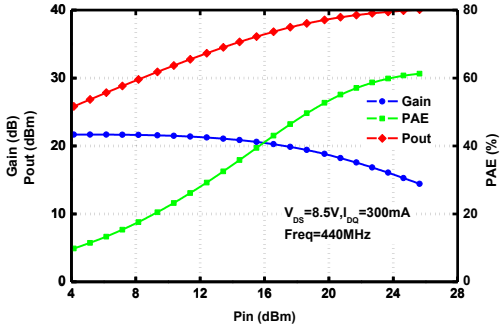
Part	Description	Part Number	Manufacturer
R1	1KOhm	—	—
L2,L3	1nH	—	—
L1	8 Turns D: 0.5 mm, φ 2.4 mm Enamel Wire	—	—
C1, C3,C4,C6,C9	100pF Chip Capacitors	GQM21P5C1H101JB01	Murata
C2, C5	39pF Chip Capacitors	GRM1885C1H201JA01	Murata
C7,C10	1000pF Chip Capacitors	GRM1885C1H102JA01	Murata
C8,C11	10uF,10VChip Capacitors	—	—
C12	10pF Chip Capacitors	—	Murata
PCB	FR-4 ,0.030”,Ɛ,4.5	—	—

TYPICAL CHARACTERISTICS

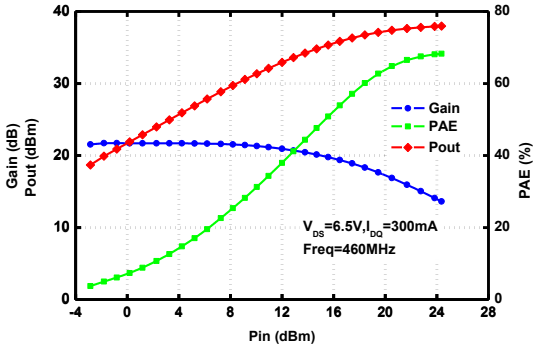
1. 440MHz @ V_{DS}, Pout, Gain, PAE vs. Pin

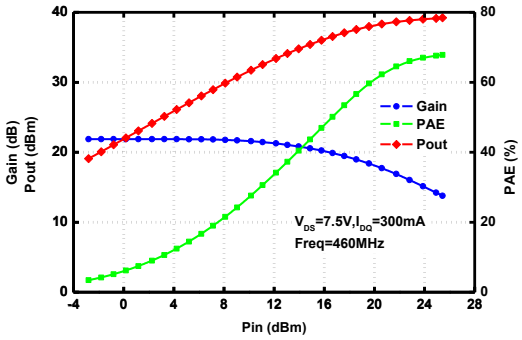


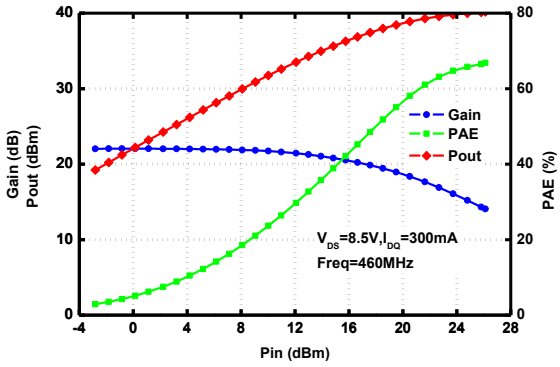




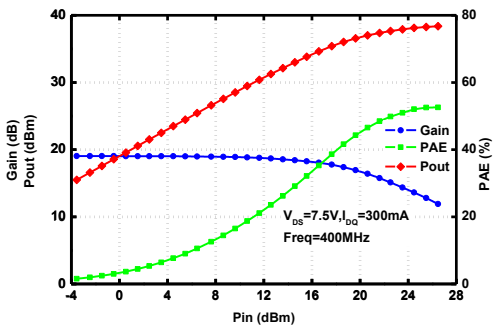
2. 460MHz @ V_{DS}, Pout, Gain, PAE vs. Pin

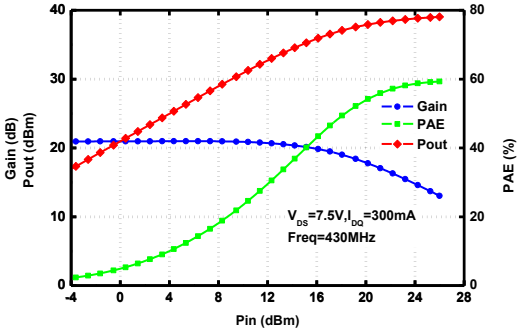


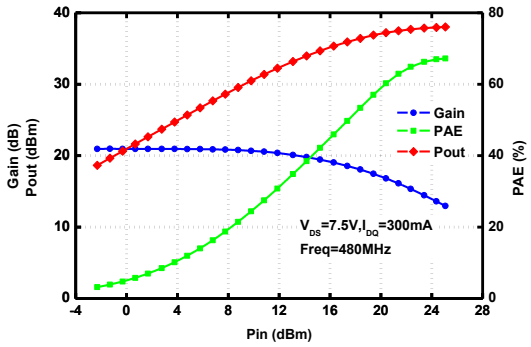


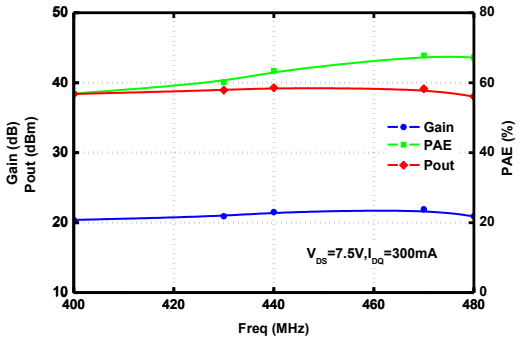


3. 7.5V @ Frequency, Pout, Gain, PAE vs. Pin



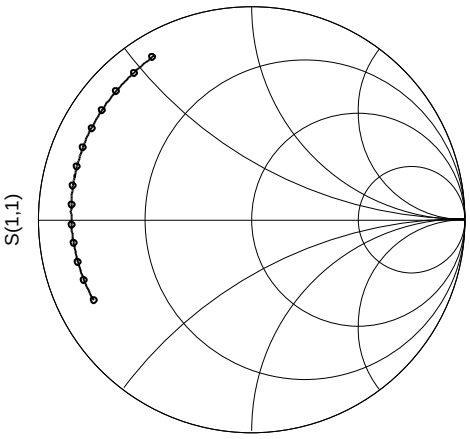




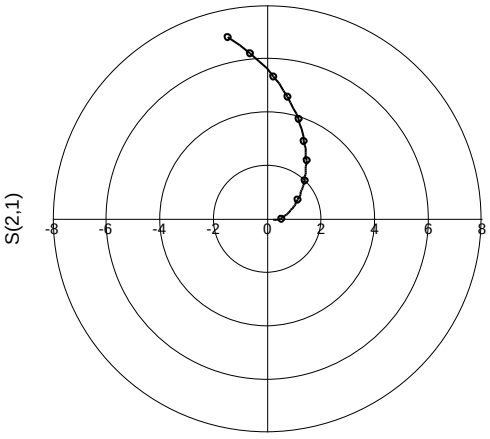


S Parameter Graph

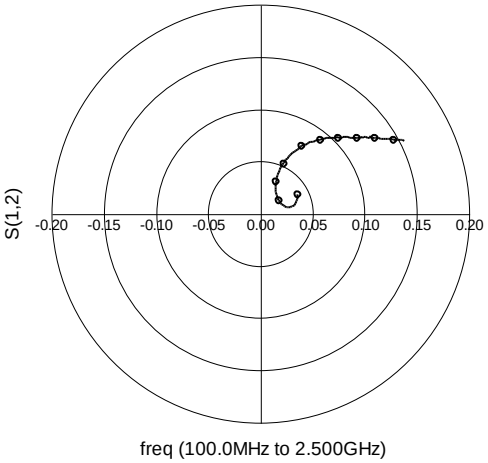
S11 vs. Frequency



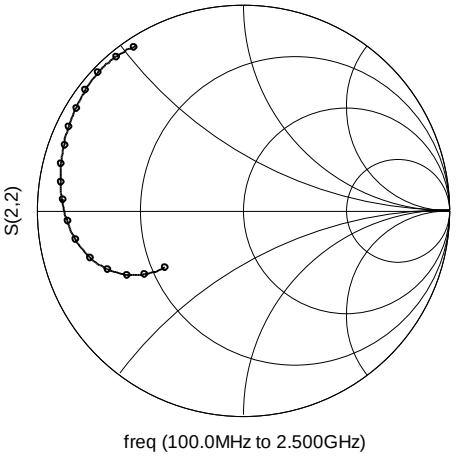
S21 vs. Frequency



S12 vs. Frequency



S22 vs. Frequency

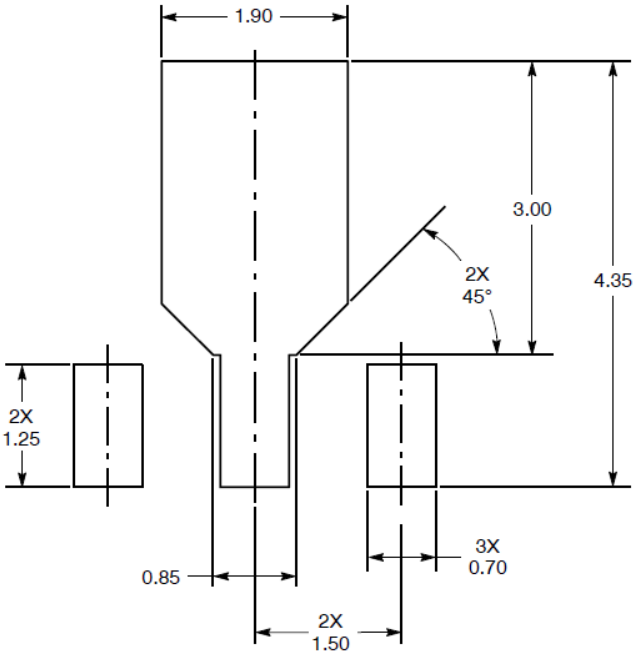


Test condition: V_{DS} = 7.5 V, I_{DQ} = 300 mA, Z_O = 50 Ω, 100 to 2500 MHz (50 MHz step).

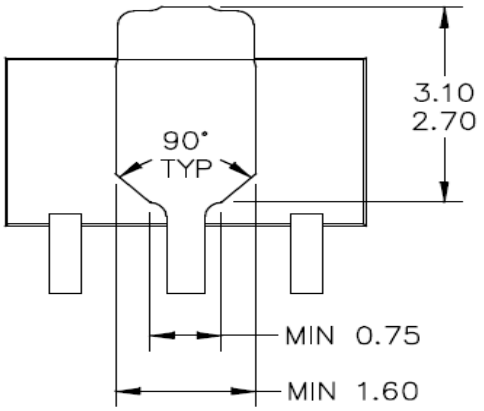
S Parameter Table (V_{DS} = 7.5 V, I_{DQ} = 300 mA, Zo = 50Ω)

f(MHz)	S11		S21		S12		S22	
	MAG	ANG(deg.)	MAG	ANG(deg.)	MAG	ANG(deg.)	MAG	ANG(deg.)
200	0.834	-152.8	6.934	102.3	0.040	28.5	0.471	-144.0
250	0.835	-158.5	5.318	87.4	0.036	19.0	0.546	-146.1
300	0.837	-162.2	4.238	76.3	0.032	14.2	0.602	-148.6
350	0.838	-165.2	3.459	67.6	0.029	12.7	0.647	-151.0
400	0.839	-167.7	2.887	60.2	0.026	14.3	0.681	-153.5
450	0.841	-170.4	2.454	53.5	0.023	18.8	0.713	-156.0
500	0.842	-172.9	2.114	47.7	0.022	25.5	0.738	-158.3
550	0.843	-175.3	1.818	42.2	0.021	35.1	0.762	-160.7
600	0.845	-177.3	1.616	38.2	0.022	43.5	0.780	-162.8
650	0.846	-179.6	1.433	33.9	0.024	51.3	0.796	-165.1
700	0.847	178.2	1.282	29.9	0.027	57.4	0.812	-167.5
750	0.848	176.0	1.155	26.3	0.030	61.6	0.826	-169.7
800	0.850	173.7	1.041	22.6	0.034	64.5	0.839	-172.2
850	0.851	171.7	0.946	19.4	0.038	66.2	0.849	-174.7
900	0.852	169.4	0.865	16.3	0.042	66.8	0.859	-177.3
950	0.854	167.3	0.797	13.4	0.046	66.8	0.870	-179.7
1000	0.855	167.3	0.735	10.8	0.051	66.5	0.879	175.8
1050	0.856	163.2	0.680	8.1	0.055	65.4	0.887	175.2
1100	0.857	161.2	0.634	5.7	0.059	64.3	0.893	172.7
1150	0.859	159.0	0.585	3.2	0.064	63.1	0.902	169.8
1200	0.860	157.0	0.545	1.1	0.068	61.6	0.908	167.5
1250	0.861	155.1	0.509	-0.8	0.072	60.2	0.916	164.9
1300	0.863	153.2	0.476	-2.6	0.076	58.6	0.921	162.3
1350	0.864	151.1	0.446	-4.6	0.080	56.5	0.927	159.7
1400	0.865	149.2	0.419	-6.2	0.084	54.6	0.935	157.4
1450	0.867	147.4	0.393	-7.4	0.087	53.3	0.939	155.3
1500	0.868	145.4	0.368	-8.9	0.091	51.4	0.945	152.8
1550	0.869	143.8	0.349	-9.8	0.094	50.0	0.948	150.9
1600	0.871	142.0	0.329	-10.7	0.097	48.3	0.953	148.9
1650	0.872	140.4	0.312	-11.4	0.100	46.7	0.957	147.1
1700	0.873	138.8	0.295	-11.9	0.103	45.2	0.958	145.4
1750	0.875	137.2	0.280	-12.5	0.105	43.7	0.962	143.6
1800	0.876	135.7	0.268	-12.6	0.108	42.5	0.967	142.3
1850	0.877	134.2	0.257	-12.8	0.111	41.2	0.969	140.8
1900	0.878	133.0	0.247	-12.8	0.114	39.9	0.972	139.4
1950	0.880	131.7	0.237	-12.5	0.116	38.9	0.971	138.3
2000	0.881	130.4	0.230	-12.3	0.119	37.9	0.970	137.0
2050	0.882	129.3	0.222	-11.9	0.122	36.8	0.976	135.8
2100	0.884	128.2	0.218	-11.5	0.125	35.7	0.975	134.7
2150	0.885	127.4	0.213	-11.0	0.128	34.7	0.974	133.5
2200	0.886	126.2	0.209	-10.6	0.131	33.6	0.973	132.5
2250	0.888	125.0	0.206	-10.2	0.135	32.4	0.973	131.1
2300	0.889	124.3	0.203	-9.8	0.138	31.5	0.973	129.8
2350	0.890	123.3	0.201	-9.3	0.142	30.5	0.969	128.5
2400	0.891	122.6	0.200	-9.0	0.145	29.4	0.965	126.7
2450	0.893	121.7	0.199	-8.7	0.149	28.3	0.961	125.2
2500	0.894	120.6	0.200	-8.5	0.154	27.1	0.955	123.2

PACKAGE

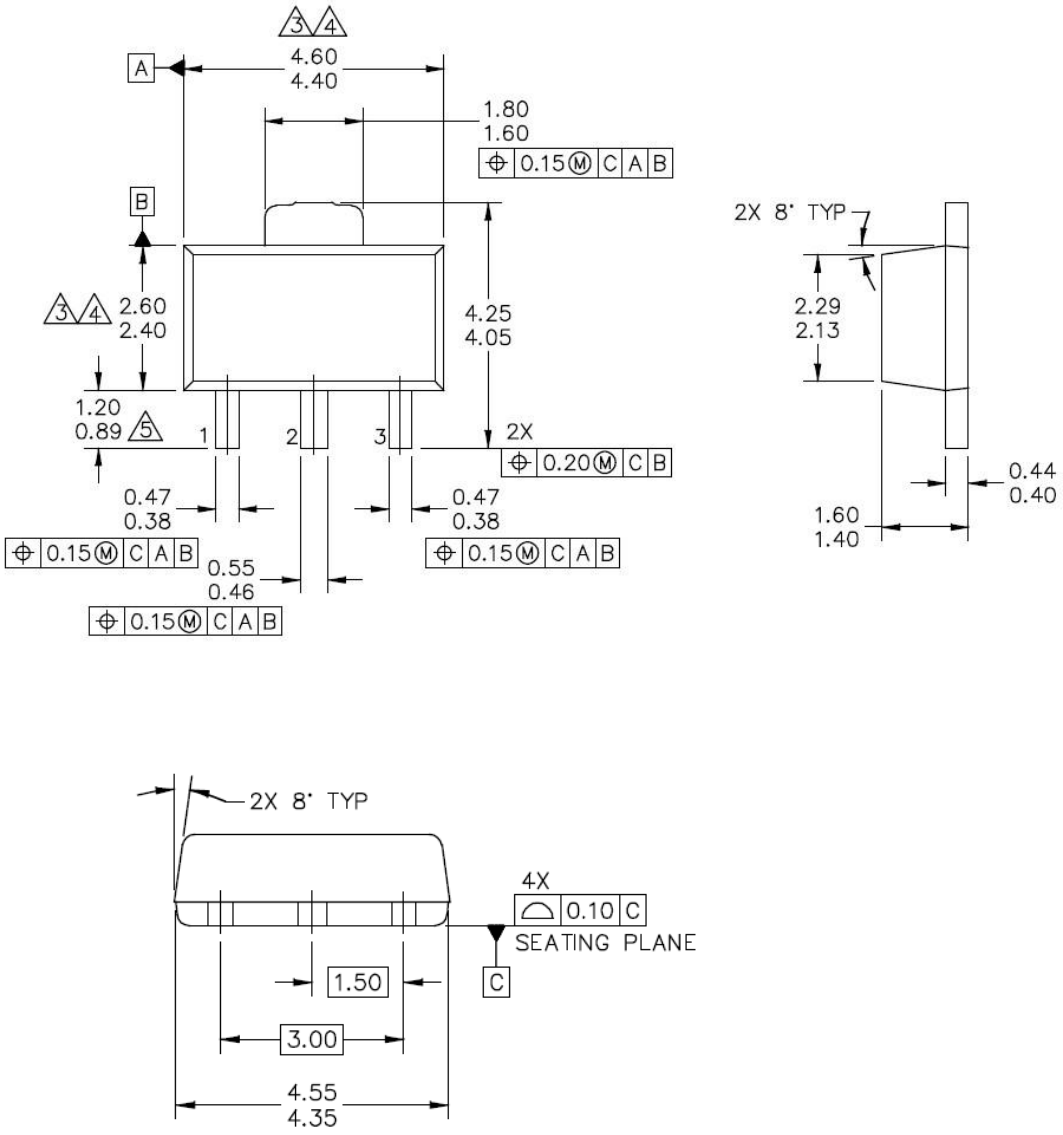


PCB Pad Layout for SOT– 89



Bottom View

PACKAGE DIMENSIONS



REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
1	May 2018	Initial Release of Data Sheet